**Processor Design Report**

The purpose of this document is to explain your processor design and the process you went through to produce it. It is composed of four segments: Construction; Implementation; Integration; and Process.

\* Required

* 1. Name \*

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

* 1. Net ID \*

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* 1. Honor Code: I have neither given nor received unauthorized help in completing this assignment and I have conducted myself within the guidelines of the Duke Community Standard. \*

*Mark only one oval.*

Yes \_\_\_\_\_\_\_\_\_

No \_\_\_\_\_\_\_\_\_

# Construction

This aspect considers the logical soundness of your processor.

* 1. How do you determine a branch should occur for bne? (200 characters max) \*

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* 1. How do you determine a branch should occur for blt? (200 characters max) \*

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# Implementation

This aspect considers efficiency, cost, simplicity, and elegance of your processor.

* 1. What is the slowest instruction in your processor? Explain why you know this. (200 characters max) \*

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1. Estimate your processor's maximum clock speed in ns (i.e. the fastest clock speed that allows the slowest instruction to correctly execute). \*

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1. Prove the above clock estimation by attaching a waveform of your processor functioning at this speed. \*

Files submitted: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# Integration

This aspect considers how well you tie together your memory elements, regfile, ALU, and other elements.

1. What clocking scheme does your processor follow, i.e., how is each clocked element in your design clocked? \*

*Check all that apply.*

PC Register Positive edge? \_\_\_\_\_\_ Negative edge? \_\_\_\_\_\_\_

Regfile Positive edge? \_\_\_\_\_\_ Negative edge? \_\_\_\_\_\_\_

Dmem Positive edge? \_\_\_\_\_\_ Negative edge? \_\_\_\_\_\_\_

Imem Positive edge? \_\_\_\_\_\_ Negative edge? \_\_\_\_\_\_\_

1. Why did you choose the above clocking scheme? (200 characters max) \*

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1. What module(s) do you use to compute the next PC? \*

*Check all that apply.*

ALU \_\_\_\_\_\_\_\_\_\_\_\_\_

32 bit Adder \_\_\_\_\_\_\_

Other: \_\_\_\_\_\_\_\_\_\_\_\_

1. Regarding the question above, why did you choose these modules for computing the next PC? (200 characters max) \*

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# Process

This aspect considers how you went about designing the processor, i.e. you own work ethic and operations.

1. How did you prepare your processor design? Ex. You created an initial visual model through Logisim or by hand, you broke down the processor into modules you wanted to design, etc. (200 characters max) \*

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1. Which of the following testing methods did you use throughout your design process? (Select all that apply) \*

*Check all that apply.*

Waveform tests of single modules \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Personally created testbenches for single modules \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Waveform tests of subgroups of modules \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Personally created testbenches for subgroups of modules \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Waveform tests of cumulative processor design \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Personally created testbenches for cumulative processor design \_\_\_\_\_\_\_\_\_

Independent web research and resolution of error/warning messages \_\_\_\_\_

Other: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. Describe one time when you found a bug in your processor: how did you find, isolate, and resolve it? (300 characters max) \*

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